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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,097	02/13/2004	Jae-jun Moon	Q77183	4555

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EXAMINER	
ZWEIZIG, JEFFERY SHAWN	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 03/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,097	MOON ET AL.	
	Examiner	Art Unit	
	Jeffrey S. Zweizig	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 2-4 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Referring first to claim 1, as best understood, the bias circuit part is directed toward Fig. 7 wherein the common node is directed toward N71 and the "MOS transistors" are directed toward MP71 and MP72. Dependent claim 2 indicates that the bias circuit part additionally includes first and second PMOS transistors. However, the first and second PMOS transistors are not additional components, they merely provide further definition to the previously defined "MOS transistors". There is no support in the disclosure for a circuit comprising both "MOS transistors" and first and second PMOS transistors as defined in claim 2. Claim 2 should be modified to clearly indicate that the first and second PMOS transistors form the previously defined "MOS transistors". For example, --wherein the first PMOS transistor and the second PMOS transistor form the MOS transistors-- could be added to claim 2. Claim 2 is not properly enabled.

As best understood, claims 3 and 4 are directed toward Fig. 13 (and possibly Fig. 14) and page 15 of the specification. Applicants have continuously argued that

Examiner's art rejections should be withdrawn because Examiner's relied upon references allegedly do not disclose "output nodes". By Applicant's own logic, claims 3 and 4 are not properly enabled because no "output node" has been disclosed in Figs 13 and 14. Nor is there any mention of an "output node" found in the description of Figs. 13 and 14. Therefore the disclosure does not support the "output node" recited in claims 3 and 4. Claims 3 and 4 are not properly enabled.

Referring to claim 3, as best understood, the bias circuit part is directed toward Fig. 13 wherein the first common node is directed toward N91 and the first MOS transistors are directed toward MP91 and MP92. Dependent claim 4 indicates that the bias circuit part additionally includes first and second PMOS transistors. However, the first and second PMOS transistors are not additional components, they merely provide further definition to the previously defined fist MOS transistors. There is no support in the disclosure for a circuit comprising both first MOS transistors and first and second PMOS transistors as defined in claim 4. Claim 4 should be modified to clearly indicate that the first and second PMOS transistors form the previously defined first MOS transistors. For example, --wherein the first PMOS transistor and the second PMOS transistor form the first MOS transistors-- could be added to claim 4. Claim 4 is not properly enabled.

Referring again to claim 3, as best understood, the bias circuit part is directed toward Fig. 13 wherein the second common node is directed toward N92 and the second MOS transistors are directed toward MP93 and MP94. Dependent claim 4 indicates that the bias circuit part additionally includes third and fourth PMOS

transistors. However, the third and fourth PMOS transistors are not additional components, they merely provide further definition to the previously defined second MOS transistors. There is no support in the disclosure for a circuit comprising both second MOS transistors and third and fourth PMOS transistors as defined in claim 4. Claim 4 should be modified to clearly indicate that the third and fourth PMOS transistors form the previously defined second MOS transistors. For example, --wherein the third PMOS transistor and the fourth PMOS transistor form the second MOS transistors-- could be added to claim 4. Claim 4 is not properly enabled.

Applicants' Appeal Brief arguments regarding claim 4 are based on a defective claim 4. Referring again to Fig. 13, as best understood, the first PMOS transistor is directed toward MP91, the second PMOS transistor is directed toward MP92, the third PMOS transistor is directed toward MP93, the fourth PMOS transistor is directed toward MP94, the first NMOS transistor is directed toward MN95 and the second NMOS transistor is directed toward MN96. As shown in Fig. 13, the gate of the fourth PMOS transistor MP94 is connected to the gate of the third PMOS transistor MP93, not the gate of the first PMOS transistor MP91 as recited in claim 4. There is no support in the disclosure for connecting the gate of the fourth PMOS transistor MP94 to the gate of the first PMOS transistor MP91. Claim 4 is not properly enabled.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 3 remain rejected under 35 U.S.C. 102(b) as being anticipated by Wu et al. (USPN 5,307,007).

Fig. 1 discloses a bias circuit part M1-M4/R1, an output node (node between M1 & M3), a start-up capacitor C1, a common node (gates of M1/M2) and MOS transistors M1/M2 as recited in claim 1.

Fig. 3 discloses a bias circuit M1-M8/R1, an output node (node between M5 & M7, a first common node (gates of M3/M4), first MOS transistors M3 & M4, a second common node (gates of M5/M6), second MOS transistors M5 & M6, a fist capacitor C1 and a second capacitor C2 as recited in claim 3.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. in view of Applicant's Prior Art Fig. 1.

Applicant has continuously argued that the Wu et al. and Yamazaki rejections should be withdrawn because the references allegedly do not show an "output node". Examiner continues to disagree with Applicant's position on this issue, however, this new grounds of rejection has been added for the sake of completeness.

Fig. 1 discloses a bias circuit part M1-M4/R1, an output node (node between M1 & M3), a start-up capacitor C1, a common node (gates of M1/M2) and MOS transistors M1/M2 as recited in claim 1. Applicant argues that the node between M1 and M3 is allegedly not an output node. Applicant's Prior Art Fig. 1 discloses a similar current source circuit including a transistor MN13 analogous to Wu et al. transistor M3 and an output node REF. It would have been obvious to one of ordinary skill in the art at the time of the invention to add an output node REF as taught by Applicant's Prior Art Fig. 1 to the drain of M3 for the benefit of conveying an output signal to the next circuit M5/M6 as shown. Claim 1 is obvious.

Fig. 3 discloses a bias circuit M1-M8/R1, an output node (node between M5 & M7, a first common node (gates of M3/M4), first MOS transistors M3 & M4, a second common node (gates of M5/M6), second MOS transistors M5 & M6, a fist capacitor C1 and a second capacitor C2 as recited in claim 3. Applicant argues that the node between M5 and M7 is allegedly not an output node. Applicant's Prior Art Fig. 1 discloses a similar current source circuit including a transistor MN13 analogous to Wu et al. transistor M7 and an output node REF. It would have been obvious to one of ordinary skill in the art at the time of the invention to add an output node REF as taught

by Applicant's Prior Art Fig. 1 to the drain of M7 for the benefit of conveying an output signal to the next circuit M9/M10 as shown. Claim 3 is obvious.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. in view of Applicant's Prior Art Fig. 1 or Yamazaki (USPN 5,180,967).

Wu et al. Fig. 1 further discloses a first PMOS M1, a second PMOS M2, a first NMOS M3, a second NMOS M4 and a resistor R1 as recited in claim 2. Resistor R1 is connected to the source of the first PMOS transistor M1 as opposed to the source of the second NMOS transistor M4 as recited in claim 2. The resistor configuration of Wu et al. Fig. 1 more closely resembles Applicant's Fig. 12 whereas claim 2 is more directed toward Applicant's Fig. 7. However, as pointed out in paragraph [57] of Applicant's specification, Figs. 7 and 12 are operationally the same. Indeed, these are simply two know variations of a known current source configuration. See, for example, Applicant's Prior Art Fig. 1 or Yamazaki Fig. 1. It would have been obvious to one of ordinary skill in the art at the time of the invention to move the resistor R1 from the source of the first PMOS transistor to the source of the second NMOS transistor as taught by Applicant's Prior Art Fig. 1 or Yamazaki Fig. 1 for the benefit of providing an alternate equivalent circuit layout. Claim 2 is obvious.

8. Claims 1-4 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Wu et al..

Yamazaki Fig. 1 discloses a bias circuit part 104/106/110/112/114, an output node (N11 or N12), a common node (gates of 104/106) and MOS transistors 104/106 as recited in claim 1. Further shown are start-up circuits 118 & 120. Not shown is a start-up capacitor as recited in claim 1. As indicated in the 102 rejections above, Wu et al. Fig. 1 (as well as Figs. 2, 4 & 6) disclose similar bias circuit parts including an output node, a common node and MOS transistors as well as start up capacitors C1 and C2. It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the Yamazaki start-up circuits 118 & 120 with a start-up capacitor as taught by Wu et al. for the benefit of reducing component count and static current consumption. Claim 1 is obvious.

Yamazaki Fig. 1 further discloses a first PMOS 106, a second PMOS 104, a first NMOS 110, a second NMOS 112 and a resistor 114 as recited in claim 2. Both N11 and N12 are valid output nodes. Yamazaki extracts a signal from the output node between the second PMOS transistor 104 and the second NMOS transistor 112, however, Wu et al. Fig. 1 shows that a signal can just as well be extracted from the output node between the first PMOS transistor M1 and the first NMOS transistor M3. Claim 2 is obvious.

Yamazaki Fig. 5 discloses a bias circuit 104/106/124/126/130/128/114, an output node (nodes between 126 & 110 or between 124 &112), first MOS transistors 104 & 106 and second MOS transistors 124 & 126 as recited in claim 3. Further shown are start-up circuits 118 & 120. Not shown are start-up capacitors as recited in claim 3. As indicated in the 102 rejections above, Wu et al. Fig. 3 (as well as Fig. 5) disclose similar

bias circuits including an output node, and MOS transistors as well as start up capacitors C1 and C2. It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the Yamazaki start-up circuits 118 & 120 with start-up capacitors as taught by Wu et al. for the benefit of reducing static current consumption. Claim 3 is obvious.

Yamazaki Fig. 5 further discloses a first PMOS 106, a second PMOS 104, a third PMOS 126, a fourth PMOS 124, a first NMOS 110, a second NMOS 112 and a resistor 114 as recited in claim 4. Nodes between 126 & 110 or between 124 &112 are all valid output nodes. For example, Wu et al. Fig. 3 shows that a signal can be extracted from an output node formed by the drain of the first NMOS transistor M7. Claim 4 is obvious.

Response to Arguments

9. Examiner has reopened prosecution primarily to address the circuit connection defect in claim 4. While it is Examiner's responsibility to catch such errors, it is sad that Applicants would chose to base an appeal argument on a circuit connection that clearly does not exist. Examiner has also taken this opportunity to shore up his position on Applicant's "output node" argument, which is a meaningless point of terminology semantics. But to ensure that Examiner's position is crystal clear, refer to the Wu et al. reference one more time. Fig. 1 shows a transistor M3 with a drain and gate connected to the drain of transistor M1. This connection is called a node. Note the small dots that define this connection, which are often referred to by those of ordinary skill in the art as "node dots". The connection between transistors M1 and M3 provides a signal to the

gates of transistors M5 and M6. Provide is another word for output. In other words, a signal is output from the node connecting M1 and M3. Those of ordinary skill in the art would refer to such a node as an output node.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey S. Zweizig whose telephone number is (571) 272-1758. The examiner can normally be reached on Monday thru Wednesday 6:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit 2816

JZ